What is claimed is:

Claims

1. In a system for processing a semiconductor wafer through plasma etching operations, the system including a process chamber having a support chuck for holding the semiconductor wafer and a pair of RF power sources; the system comprising:

an electrode being positioned within the system and over the semiconductor wafer, the electrode having a center region, a first surface and a second surface, the first surface is configured to receive processing gases from a source that is external to the system and flow the processing gases into the center region, the second surface has a plurality of gas feed holes that are continuously coupled to a corresponding plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings are configured to define an electrode surface that is defined over a wafer surface of the semiconductor wafer.

2. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 1, wherein the electrode is coupled to one of the pair of RF power sources and the support chuck is coupled to the other one of the pair of RF power sources.

3. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 2, wherein a plasma is defined between the second surface of the electrode and the wafer surface.

4. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 3, wherein a first plasma sheath is defined next to the wafer surface and a second plasma sheath is defined next to the second surface, and the second plasma sheath follows an outline defined by the electrode openings of the second surface of the electrode.

5. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 4, wherein the first plasma sheath has a first area and the second plasma sheath has a second area, and the second area of the second plasma sheath is larger than the first area of the second plasma sheath.

6. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 1, wherein the electrode openings are at least about 5 mm or greater in diameter and the gas feed holes have a diameter of about 1 mm.

7. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 6, wherein a separation of between about 0.75 cm and about 4 cm is defined between the electrode surface and the wafer surface.

8. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 1, wherein two or more gas buffer plates are contained within the center region of the electrode.

9. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 1, wherein the electrode openings are defined in a hexagonal pattern arrangement throughout the second surface of the electrode.

10. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 5, wherein the second area of the second plasma sheath is between about 2 and 3 times greater than the first area of the first plasma.

11. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 10, wherein the second area of the second plasma sheath is about 2.7 times greater than the first area of the first plasma sheath.

12. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 10, wherein when the second area of the second plasma sheath is greater than the first area of the first plasma sheath, an increase in bias voltage is applied to the wafer surface and a decrease in bias voltage is applied to the second surface of the electrode.

13. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 12, wherein the increase in bias voltage causes an increase in ion bombardment energy onto the wafer surface, thereby increasing etch control.

14. In a chamber for processing a semiconductor wafer through plasma etching operations, the chamber including a support chuck for holding the semiconductor wafer and a pair of RF power sources; a method for making a top electrode for the chamber, comprising:

forming the top electrode to have a center region, a first surface and a second surface, the first surface has an inlet that is configured to receive processing gases from a source that is external to the system and flow the processing gases into the center region, the second surface has a plurality of gas feed holes that lead to a plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings are configured to define an electrode surface that is defined over a wafer surface of the semiconductor wafer.

15. The method for making a top electrode for the chamber as recited in claim 14, further comprising:

coupling the top electrode to one of the pair of RF power sources and the support chuck to the other one of the pair of RF power sources.

16. The method for making a top electrode for the chamber as recited in claim 15, further comprising:

forming the electrode openings to be at least about 5 mm or greater in diameter and the gas feed holes to have a diameter of about 1 mm.

17. The method for making a top electrode for the chamber as recited in claim 15, further comprising:

defining the electrode openings to a depth of between about 1/32 inch and ¼ inch.

18. The method for making a top electrode for the chamber as recited in claim 16, further comprising:

fixing a separation of between about 0.75 cm and about 4 cm between the electrode surface and the wafer surface.

19. The method for making a top electrode for the chamber as recited in claim 18, further comprising:

inserting two or more gas buffer plates within the center region of the top electrode.

20. The method for making a top electrode for the chamber as recited in claim 18, further comprising:

striking a plasma between the separation, the plasma having a first plasma sheath that is proximate to the wafer surface and a second plasma sheath that outlines an inner region of the top electrode openings, such that the second plasma sheath has an area that is greater than the first plasma sheath.

21. The method for making a top electrode for the chamber as recited in claim 20, further comprising:

increasing an ion bombardment energy over the wafer surface when the second plasma sheath has the area that is greater than the first plasma sheath.

22. A plasma process chamber for processing a semiconductor wafer, the plasma process chamber including a support chuck for holding the semiconductor wafer and a pair of RF power sources, the plasma process chamber, comprising:

an electrode means for providing gas chemistries into a process region that is defined between the electrode means and a wafer surface of the semiconductor wafer, the electrode means having a plurality of oversized gas feed holes that are configured to define an electrode surface over the wafer surface; and

wherein when a plasma is generated between the electrode surface and the wafer surface in the plasma process chamber, a substantially planar first plasma sheath is defined over the wafer surface and a contoured second plasma sheath is defined over the electrode surface, such that the contoured second plasma sheath

extends into the plurality of oversized gas feed holes, and therefore the contoured second plasma sheath has a greater surface area than the substantially planar first plasma sheath.

23. A plasma process chamber for processing a semiconductor wafer as recited in claim 22, wherein the oversized gas feed holes are arranged in a hexagonal pattern throughout the electrode surface.

24. A plasma process chamber for processing a semiconductor wafer as recited in claim 23, wherein each of the oversized gas feed holes have a diameter that is set to be about 5 mm or greater.

25. A plasma process chamber for processing a semiconductor wafer as recited in claim 22, wherein when the contoured second plasma sheath has a greater surface area than the substantially planar first plasma sheath, an increased bias voltage is generated over the wafer surface and a decreased bias voltage is generated over the electrode surface.

26. A plasma process chamber for processing a semiconductor wafer as recited in claim 25, wherein the increase in bias voltage over the wafer surface causes in increase in ion bombardment energy over the wafer surface and an increase in etch control of high aspect ratio features.

27. In a system for processing a semiconductor wafer through plasma etching operations, the system including a process chamber having a support chuck for supporting the semiconductor wafer and having a RF power source connected thereto; the system comprising:

a grounded electrode being positioned within the system and over the semiconductor wafer, the grounded electrode having a center region, a first surface and a second surface, the first surface is configured to receive processing gases from a source that is external to the system and flow the processing gases into the center region, the second surface has a plurality of gas feed holes that are continuously coupled to a corresponding plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings are configured to define an electrode surface that is defined over a wafer surface of the semiconductor wafer.

28. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 27, wherein a plasma is defined between the second surface of the electrode and the wafer surface.

29. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 28, wherein a first plasma sheath is defined next to the wafer surface and a second plasma sheath is defined next to the second surface,

and the second plasma sheath follows an outline defined by the electrode openings of the second surface of the electrode.

30. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 29, wherein the first plasma sheath has a first area and the second plasma sheath has a second area, and the second area of the second plasma sheath is larger than the first area of the second plasma sheath.

31. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 27, wherein the electrode openings are at least about 5 mm or greater in diameter and the gas feed holes have a diameter of about 1 mm.

32. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 30, wherein when the second area of the second plasma sheath is greater than the first area of the first plasma sheath, an increase in bias voltage is applied to the wafer surface and a decrease in bias voltage is applied to the second surface of the electrode.

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